Design of an EEG Preamplifier for Brain-Computer Interface

Xian-Jie Pu, Tie-Jun Liu, and De-Zhong Yao

Abstract—As a non-invasive neurophysiological index for brain-computer interface (BCI), electroencephalogram (EEG) attracts much attention at present. In order to have a portable BCI, a simple and efficient pre-amplifier is crucial in practice. In this work, a preamplifier based on the characteristics of EEG signals is designed, which consists of a highly symmetrical input stage, low-pass filter, 50 Hz notch filter and a post amplifier. A prototype of this EEG module is fabricated and EEG data are obtained through an actual experiment. The results demonstrate that the EEG preamplifier will be a promising unit for BCI in the future.

Index Terms—Brain-computer interface (BCI), electroencephalogram (EEG), filtering, interference, preamplifier.

1. Introduction

Electroencephalogram (EEG) is generated by neural activities within brain and may ultimately shed light on the inner works of brain with its highly temporal resolution. Born in the brain science research, brain-computer interface (BCI) has been developed to serve severely disabled individuals or the entertainment[1], [2], and EEG is the optimal measure[3]-[5] to realize this flourishing technology for its strongpoint thereinafter: noninvasive, convenient acquisition and low cost, etc. Studies of the past 30 years show that the brain signals used for BCI could be classified into three groups: the exogenous signals such as steady-state visual evoked potential (SSVEP)[6] and P300 components[2], [7], the endogenous signals such as μ and β rhythms (i.e., sensorimotor rhythms, SMRs)[2], α-waves[8],[9], and the modulated responses such as slow cortical potential (SCP)[10].

In EEG acquisition system, preamplifier is the most crucial part. EEG signals recorded from the human brain by the placement of electrodes on the surface of the scalp are very small (on the order of a few microvolts). Hence, an amplification module is required to amplify these small potentials to an acceptable level. Further, due to the small amplitude, these signals are very susceptible to any interference introduced through body, amplifier, measurement cables and magnetically induction as described in [11]. Moreover, the DC voltage owing to the polarization of electrodes and the noise caused by power supply are also serious in bio-potential measurements. So a signal conditioning circuit is required which is capable of filtering certain high and low frequency components of the input while allowing only the signal in the desired bandwidth to pass[12]. An actual preamplifier should include these parts discussed above, and it is also the foremost unit in an EEG recording system for a purified true EEG signal converted into a digital form.

The channel numbers for actual BCI implementing are usually not as many as in clinics or some other psychological applications. The BCI community recently focuses on converting the current complex systems used in the laboratory into practical user-friendly ones[2]. In this work, a single-channel EEG preamplifier was developed, oriented to the later construction of an online BCI system.

2. Circuit Design

The configuration of the system is shown in Fig. 1. Weak EEG signals picked up by the electrodes are conditioned suitable for analog-to-digital conversion after filtering and amplifying. The dashed block is the main part to be considered in this work. To power this EEG module, the recommended way is by a 9 V or 12 V battery[13], and in this work the off-the-shelf 9 V battery is chosen.

![Fig. 1. Block diagram of the EEG preamplifier.](image-url)
2.1 Input Stage

A. Instrument amplification and DC block

Although the monolithic instrumentation amplifier with highly symmetric could reduce the active devices used to form a three op-amp structure to get high input impedance and good common-mode rejection, there are still some situations in which it is not as flexible as the classic three op-amp approach because it is fixed. In real application of EEG acquisition, the sensors are typically made of metal and they contact with the skin through an electrically-conductive gel\(^\text{[14]}\). The electrode-skin interfaces are considered to be a possible source of excess noise: both the gelled surface of the electrode (metal/electrolyte) and the interface from gel to skin (electrolyte/electrolyte) may act like a voltaic cell (so-called polarized voltage). Even though the developed voltages at the two electrodes have opposite polarity and should partly cancel each other, poor balance may result in residual noise\(^\text{[15]}\). This could make the amplifier saturated without DC block in the front-end circuit. One solution is to introduce a high-pass filter in front of instrumentation amplifier, but the cost is the decrease of the input impedance.

The forefront adopts a dual op-amp OPA2277 with the features as high open-loop gain, high impedance and high CMRR to construct the first stage in the form of parallel connected noninverting amplifier as shown in Fig. 2. Because the two op amps in the same chip have identical characteristics, some degradation of CMRR due to component mismatch could be avoided. The gain of the first amplifier stage should not be too high, and in this design it is set as \(G_1 = 1 + 2R_4 / R_2 = 41\)\(^\text{[16]}\). Capacitors \(C_{13}\) and \(C_{16}\), and resistors \(R_{10}\) and \(R_{11}\) compose the DC block circuit with a cutoff-frequency of \(f_c = 1/(2\pi R_{10} C_{17}) = 0.07\) Hz\(^\text{[16]}\), which can not be implemented in the instrumentation amplifier. The differential amplification stage is fulfilled by the packed instrumentation amplifier (AD620, high open-loop gain, high impedance and high CMRR, etc.). The gain is programmed accurately with a single external resistor as \(G = \frac{49.4\ \text{k} \Omega}{R_2} + 1\), where \(R_2\) is \(R_{23}\). If \(R_{23}\) is adjusted between 1 k\(\Omega\) and 10 k\(\Omega\), the gain of the second amplifier stage \(G_2\) (i.e., \(G\) in the latest equation) will vary from 6 to 50, then the gain of the input stage could be modulated from 246 to 2050.

B. Common-Mode Driving Circuit

The common-mode driving circuit, as shown in Fig. 2, is constructed by two equivalent resistors \(R_3\) and \(R_6\), as well as the voltage follower U2A. Marking the outputs of op amps U1A and U1B as \(V_{o1}\) and \(V_{o2}\) respectively, and \(V_c\) the input of op amp U2A, then \(V_c = 1/2(V_{o1} + V_{o2})\)\(^\text{[16]}\). As differential-mode signal inputs only (i.e., \(V_{o1} = -V_{o2}\)), the midpoint voltage \(V_c = 0\), then the output of U2A is zero; as differential-mode signal and common-mode signal input simultaneously, the output of U2A only contains the common-mode part of the input signals. It means that the common-mode signal could be input to the instrumentation amplifier directly instead of being translated to differential-mode disturbance for the mismatch of the components in RC coupling circuit\(^\text{[16]}\).

C. Driven right leg circuit

The common-mode voltage fetched by the common-mode driving circuit is feedback to “right leg” after the phase inverter U2B. Here the “right leg” is assumed at the \(C_2\) position in the International 10-20 system for scalp electrode placement\(^\text{[17]}\). This negative feedback loop reduces the common-mode voltage input and improves the capacity to resist power line interference. High resistance \(R_3\) could secure the subject when high voltages between the body and the ground occur\(^\text{[16]}\).

2.2 Low-Pass Filter

![Fig. 2. The schematic of input stage.](image)

![Fig. 3. Typical circuit of MAX280.](image)
The MAX280 is a 5th-order all-pole instrumentation low-pass filter. The typical circuit of the chip is shown in Fig. 3. There is an internal 140 kHz (nominal) oscillator on the chip. By connecting an external capacitor in parallel with the on-chip 33 pF capacitor (from the \( C_{osc} \) pin to GND), the clock frequency \( f_{osc} \) could be modified and is expressed as:

\[
f_{osc} = 140 \text{ kHz}(33\text{pF}/(33\text{pF} + C_{osc}))
\]  

(1)

Because of the process tolerances, \( f_{osc} \) can vary by \( \pm 19.5\% \). The oscillator frequency can be adjusted by adding a series potentiometer between the capacitor and the \( C_{osc} \) pin. The new frequency can be computed by:

\[
f'_{osc} = f_{osc}/(1 - 4R_pC_{osc}/f_{osc})
\]  

(2)

The clock to cutoff-frequency ratio is 100:1. Setting the cutoff-frequency \( f_c \) at 100 Hz, the clock frequency will be 10 kHz. According to the equalities above, \( C_{osc} \) could be set at 1000pF, and the potentiometer \( R_p \) 50 kΩ. The external resistor and capacitor are used as part of a feedback loop for the filter and also form one pole:

\[
f_c = \frac{1}{1.62 \frac{1}{2\pi RC}}
\]  

(3)

Typically, \( R \) is selected around 20 kΩ, here we set it as 25 kΩ, thus \( C \) is 0.1 μF.

### 2.3 50 Hz Notch Filter

Digital approaches have been widely adopted to solve the power line interference problems including proper grounding and electrical shielding in analog recordings\(^{[18]}\); however, the preprocessing is necessary because power line interference which overwhelms the desired signals is actually all around. This design modifies the classical twin-T notch filter to be Q-factor tunable as shown in Fig. 4.

![Circuit diagram of 50 Hz twin-T notch filter.](image)

### 2.4 Post Amplifier

EEG waves differ not only among individuals but also in varying positions on the head and correlate with their awareness levels. Therefore, a gain-tunable amplifier is configured to meet the requirements in various situations. The last stage of this design is an output inverting amplifier with a passive high-pass filter to avoid saturation as shown in Fig. 5. The gain, \( G = -(R_{22} + R_{29})/R_{20} \), adjusted by \( R_{20} \), is about 20 to 40.

![Circuit diagram of post amplifier.](image)

### 3. Circuit Performance

A prototype of the EEG preamplifier is fabricated as shown in Fig. 6. The main specifications of the preamplifier are given in Table 1. To test the validity of the EEG preamplifier working in real life, an experiment was performed in which EEG data was collected from a person, as shown in Fig. 7. The amplifier module was connected using a custom bio-potential acquisition system with the sampling rate of 200 Hz to a desktop PC. According to the International 10-20 system, float electrode was placed at the O2 position to detect the widely observed \( \alpha \)-waves, reference electrode at the T4 position, and DRL electrode at the Cz position\(^{[17]}\). In the test, the subject was asked to keep his eyes closed for several seconds, then opened for the same time. The power spectrum was calculated from the data of each section after removing the strong power interference and DC voltage by a digital filter with a pass band from 3 Hz to 35 Hz in Matlab. The test results is shown in Fig. 8. In Fig. 8 (a), a bump at 10 Hz is a result of increased \( \alpha \)-waves with eyes closed in section A. This is a typical EEG component with pronounced characteristics.
which is currently being investigated by the brain research community and adopted in BCI system without external stimuli as early as in 1967 when Dewan utilized it to transmit Morse code\cite{8}.

4. Conclusions

According to the performance test, the preamplifier described in this paper has great common-mode rejection ratio (CMRR) profiting from the highly symmetrical design of the input stage. The main flaw of this module lies in the noise generated by the clock signal inside the body, measurement cables and the amplifier itself without shielding. To improve this preamplifier, there are several approaches, such as modifying the low-pass filter design, adopting shielding measures and using SMDs to reduce the surface area.

Small-signal amplification is always a difficult problem in the field of circuit system design. The presented amplifier module proposes a way for preprocessing EEG signals. More contents about DSPs, electrode optimization, system control and data transmission etc. need to be better discussed in the next stage, and it is believed that all of them will be employed in the BCI system.

Table 1: Specifications of the amplifier

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common input impedance</td>
<td>250(\Omega)(\cdot)pF</td>
</tr>
<tr>
<td>Differential input impedance</td>
<td>100(\Omega)(\cdot)pF</td>
</tr>
<tr>
<td>CMRR</td>
<td>109.5 dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>0.1 Hz to 90 Hz</td>
</tr>
<tr>
<td>Notch depth</td>
<td>−29 dB</td>
</tr>
<tr>
<td>Input-referred noise</td>
<td>10 (\mu)V(_{p-p})</td>
</tr>
</tbody>
</table>

![Fig. 7. Frequency response plot.](image)

![Fig. 8. EEG signals after digital filtering and their power spectrums: (a) increased \(\alpha\)-waves when eyes closed and (b) \(\alpha\)-waves block after eyes opening.](image)

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References


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