Abstract—A complex programmable logical device (CPLD) based on conventional embedded Flash memory process with 72 macro cells is studied in the paper. Compared with the Flash cell array technology employed by foreign companies, this architecture exhibiting in-system reconfiguration and rapid response was manufactured by low cost fabrication process. The device architecture and critical cell design are also analyzed in detail in the paper. The CPLD was designed by full-custom ASIC technology and manufactured by 0.35 μm 3P3M Flash process with 72 macro cells and 5 V voltage supply. The measurement results indicate that the devices are able to operate above the frequency of 66.7 MHz with the pin delay less than 10 ns.

Index Terms—CPLD, Flash process, Macro cell, System frequency.

1. Introduction

The merits of easy application, predictable sequence and high speed make the CPLD widely used in logic designs. The CPLD can bring the flexibility and convenience for VLSI system design, while can greatly cut down the cycle of time-to-market for product [1].

The CPLD technology has been very mature with full family of products for some big manufacturers in the world, e.g. Xilinx, Altera and Lattice, etc. In contrast, the CPLD technology is still in the R&D stage in China. The current dominant technology adopted by foreign companies is Flash cell array, which includes a transistor for data saving and a transistor for data access.

In this architecture of CPLD, the transistor for data saving is Flash transistor. In order to ensure the working speed, etc., the design of Flash transistor is different from the Flash transistor in conventional memories. Inevitably this adds difficulties to fabrication processes, which are difficult to be transplanted.

A nonvolatile CPLD architecture is proposed in this paper, where the advantages of in-system reconfiguration, rapid response, as well as manufactured by low cost fabrication process are exhibited. MOSFET employed for the logic cell matrix makes circuit design easier, process variation insensitive and process transplantable. Other advantages include simple fabrication by embedded Flash memory process, faster speed and lower static power consumption realized by SRAM controlled NMOS.

The design of device architecture and critical cell is discussed in this paper. The devices were manufactured by Flash process. The measurement results indicate that the device performance fully satisfies the requirements of our clients.

2. CPLD Design

2.1 Architecture Design

CPLD is a complex subsystem, which consists of 3 parts as shown in Fig. 1. The first part is programmable logic, i.e. the configurable logic block (CLB), which is the assembly of 18 macro cells. The second part is I/O block. The third part is programmable interconnect array (PIA) for interconnecting configurable logic blocks and I/O blocks [2].

Fig. 1. CPLD architecture.

The CLB of product-term based CPLD is composed of product-term array, product-term assignment and macro cells. Macro cell is the building block of CLB and can achieve basic logic functions.

The functions of I/O block include control of electrical characteristics, slew rate adjusting, triple-state output, and programmable ground connection. The I/O block is also capable of providing 24 mA output current.

The PIA takes charge of signal propagation, interconnect of macro cells inside configurable logic block, and I/O block.

2.2 Programming Technology

Fabrication processes for CPLD are categorized into EEPROM and Flash process, accordingly, EEPROM and
Flash programming, both of which are able to be programmed in-system.

The Flash process and Flash programming technology are utilized in this paper. Compared with EEPROM process, the Flash process is advantageous in reliability, density and performance. In addition, Flash can be erased by blocks while the EEPROM can only be erased by a byte each time\(^3\),\(^4\). The Flash programming technology is able to satisfy the need of high density devices and to be fabricated by more advanced processes.

Physically, Flash transistor includes a polysilicon layer of floating gate, which is isolated from the substrate by a thin oxide layer. The control gate is above the floating gate, in between the insulation layer of O-N-O\(^5\). The control gate is connected to the internal logic driving circuit while the connection is not necessary for floating gate. The schematic of Flash cell and cross section are illustrated in Fig. 2.

\[ f = f_1 + f_2 + f_3 
= (IN_1 + IN_2 + IN_3) \bullet (IN_4 \bullet IN_5) \bullet IN_6 
= IN_1 \bullet IN_4 \bullet IN_5 \bullet IN_6 + IN_2 \bullet IN_5 \bullet IN_5 \bullet IN_6 
+ IN_3 \bullet IN_4 \bullet IN_5 \bullet IN_6 \]  

Choosing \( SEL=1 \) of the output of combinational logic in selectable logic block gets combinational logic. Likewise, Choosing \( SEL=0 \) of output of sequential logic in selectable logic block gets sequential logic. In other words, programmable D or T flip-flop in macro cell can be used to realize sequential logic. Clock signal CLK will be input to the special channel of internal global clock via I/O pad, directly connecting to the clock terminal of the programmable flip-flop. The output of the programmable flip-flop is directly connected the I/O. In this way, the sequential logic is realized by CPLD.

Only one macro cell is required for the circuit in Fig. 3. However, one macro cell is not enough for the case of very complex circuit. Consequently, the parallel extension and sharing extension are required to interconnect with multiple macro cells. Additionally, output of macro cell can be interconnected with PIA as input of another macro cell. In this approach, more complicated logic functions are able to be achieved.

### 3. Design of Critical Cell Circuitry

#### 3.1 Design of JTAG Cell with ISP

As shown in Fig. 5, JTAG cell is the unit for device programming, testing and verification, which consists of TAP controller, device ID, instruction decoder, ISP enable register, bypass circuit, ISP configure register, boundary scanning register and ISP control circuit\(^6\),\(^7\). JTAG is capable of boundary scanning and can provide a standard interface for in-system programming controller\(^6\).
3.2 Design of Macro Cell

Macro cell of CPLD possesses functions of configurable flip-flop and polarity control. The polarity control has the capability of realizing the ‘original’ and ‘reverse’ of an expression, allowing the logic results to be achieved by minimum product terms. Outputs of CLB can be configured as D flip-flop (D_FF), T flip-flop and combinational logic. The functions of macro cell are indicated in Fig. 6 and Table 1, while the structure and functions of the D_FF are demonstrated in Fig. 7 and Table 2.

![Fig. 6. A CPLD macro cell.](image)

### Table 1: Configuration description in micro cell to realize different functions

<table>
<thead>
<tr>
<th>( B_1 _SEL )</th>
<th>( B )</th>
<th>( B_2 )</th>
<th>( MOD )</th>
<th>( B_1 _SEL ) status and function description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>( B_1 = 0, \text{SEL}=0; ) macro cell not used</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>( B_1 = 0, \text{SEL}=0; ) as D flip-flop</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>( B_1 = 0, \text{SEL}=0; ) as T flip-flop</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>( B_1 = 0, \text{SEL}=0; ) macro cell not used</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>( B_1 = 0, \text{SEL}=0; ) as D flip-flop</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>( B_1 = 0, \text{SEL}=0; ) as T flip-flop</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>( B_1 = 1, \text{SEL}=0; ) combinational logic</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>( B_1 = 1, \text{SEL}=0; ) combinational logic</td>
</tr>
<tr>
<td>1</td>
<td>Pt_data</td>
<td>0</td>
<td>X</td>
<td>XOR logic</td>
</tr>
</tbody>
</table>

Note: \( B_1 \_SEL \) and \( B_2 \) can not go 1 simultaneously.

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3.3 Design of NOR Array Based on SRAM

Fig. 8 illustrates the implementation of NOR array based on SRAM. As depicted, the NMOS are controlled by SRAMs. There are totally 72 inputs, which are 36 complementary pairs. The product term is the NOR logic result of the 72 inputs \[^9\]. The information in SRAMs is loaded from Flash memories. When SRAM is 1, corresponding NMOS is on, whereas the NMOS is off.

![Fig. 8. NOR array based on SRAM.](image)

### Table 2: Logic description by flip-flop

<table>
<thead>
<tr>
<th>( CP )</th>
<th>( EN )</th>
<th>( S )</th>
<th>( R )</th>
<th>( D )</th>
<th>( Q )</th>
<th>( Q_N )</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
<td>X</td>
<td>0</td>
<td>1</td>
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<tr>
<td>X</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>hold</td>
<td>hold</td>
</tr>
<tr>
<td>0~1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>hold</td>
<td>hold</td>
</tr>
<tr>
<td>1~0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>D</td>
<td>D</td>
<td>--D</td>
</tr>
</tbody>
</table>

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4. Design Results

Our CPLD was manufactured by using 5 V 0.35 μm 3P3M Flash process with bridge layout and full custom ASIC technology \[^{10}\]. The die size is 6.8 mm×6.5 mm. Layout for CPLD is illustrated in Fig. 9.

Since logic functions of CPLD are programmed by users, a verification scheme was proposed to fully verify functions and parameters realized by our design. The CPLD was configured as two 8-bit adding/subtracting counters, a 25-bit frequency divider, an 8-bit comparator and a 16-bit decoder \[^{11}\]. Resource utilization rate is indicated in Table 3.
The dies were packaged by PLCC44, PLCC84 and PQFP100, etc. The measuring results indicate that the devices are able to operate above the frequency of 66.7 MHz with the pin delay less than 10 ns.

5. Conclusions

A CPLD based on conventional embedded Flash memory process with 72 macro cells is proposed in the paper. This architecture exhibiting in-system reconfiguration and rapid response was manufactured by low cost fabrication process and packaged in many types. The device architecture and critical cell design are also analyzed in detail in the paper. The measurement results indicate that the devices are able to operate above the frequency of 66.7 MHz with the pin delay less than 10 ns. Based on our CPLD architecture, 108, 144, 216 and 288 macro cells have been achieved for CPLD.

References


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