A High-Performance Operational Amplifier for High-Speed High-Accuracy Switch-Capacitor Cells

Qi Fan, Ning Ning, Qi Yu, and Da Chen

Abstract—A high-speed high-accuracy fully differential operational amplifier (op-amp) is realized based on no-Miller-capacitor feedforward (NMCF) compensation scheme. In order to achieve a good phase margin, the NMCF compensation scheme uses the positive phase shift of left-half-plane (LHP) zero caused by the feedforward path to counteract the negative phase shift of the non-dominant pole. Compared to traditional Miller compensation method, the op-amp obtains high gain and wide band synchronously without the pole-splitting effect while saves significant chip area due to the absence of the Miller capacitor. Simulated by the 0.35 µm CMOS RF technology, the result shows that the open-loop gain of the op-amp is 118 dB with the unity gain-bandwidth (UGBW) of 1 GHz, and the phase margin is 61º while the settling time is 5.8 ns when achieving 0.01% accuracy. The op-amp is especially suitable for the front-end sample/hold (S/H) cell and the multiplying D/A converter (MDAC) module of the high-speed high-resolution pipelined A/D converters (ADCs).

Index Terms—Feedforward compensation, op-amp, pipelined A/D converter, switch-capacitor.

1. Introduction

Due to the higher precision and higher sampling rate than other kinds of A/D converter (ADC), the pipelined ADC is used extensively in the realm of high-speed digital transmission, digital image processing, etc. The ever increasing speed and resolution of the pipelined ADC poses challenging requirement on the op-amp which plays an important role in the front-end sample/hold (S/H) cell and the multiplying D/A converter (MDAC) module of the ADC. The realization of high-gain wide-band op-amps is therefore very desirable[1][2].

The most commonly used op-amps for pipelined ADCs are single-stage cascode amplifiers and two-stage Miller amplifiers which schemes are shown in Fig. 1[3].

The single-stage cascode amplifier is well suitable for high-speed application for its dominant pole locates at the output node while its non-dominant poles all lie at very high frequency, and yet its output swing is usually limited[3]. The two-stage Miller amplifier can obtain large output swing and high DC gain, but the dominant pole is located inside with a low-frequency non-dominant pole at the output node. Though Miller capacitors result in pole-splitting effect which enlarges the phase margin, the dominant pole is pushed to lower frequency which decreases the gain-bandwidth obviously[4].

The proposed two-stage op-amp structure overcomes the drawbacks of the amplifiers mentioned above by employs a feedforward path to create a left-half-plane (LHP) zero without any Miller capacitor. The dominant pole is not pushed to lower frequency, resulting in a higher unity gain-bandwidth with a fast step response.

2. Feedforward Compensation Scheme

The proposed compensation scheme is shown in Fig. 2[5]. The no-Miller-capacitor feedforward (NMCF) compensation scheme does not use any compensation capacitor, but uses the LHP zeros to obtain a good phase margin. A LHP zero produced by feedforward path causes a +90º shift in the phase and is used to cancel the −90º phase shift caused by the non-dominant pole.
The main concept can be explained if single-pole responses for all the blocks are assumed. $A_{i1}$, $A_{i2}$, and $A_{i3}$ are the DC gains of the first, second, and feedforward stages of the amplifier. The pole of the first stage is located at $\omega_{p1} (=1/r_{i1}C_{o1})$ and the second and third stages have a common pole at $\omega_{p2} (=1/r_{o2}C_{o2})$. It can be easily found that the overall voltage gain transfer function is given by (1).

$$H(s) = \frac{A_{i1}A_{i2} + A_{i3}(1+s/\omega_{p1})}{(1+s/\omega_{p1})(1+s/\omega_{p2})} \frac{A_{i3}s}{(1+s/\omega_{p1})(1+s/\omega_{p2})}.$$  

(1)

The transfer function has two poles along with a LHP zero created by the feedforward path. The DC gain is given by $A_{i1}A_{i2}A_{i3}$ while the location of the LHP zero is$^{[5]}$

$$Z = -\omega_{p1}(1 + \frac{A_{i1}A_{i2}}{A_{i3}}) \approx \frac{g_{m1}}{C_{o1}} \frac{g_{m2}}{g_{m3}}.$$  

(2)

In (2), the value $g_{m1}/C_{o1}$ stands for the unity gain-bandwidth of the first stage approximately. Noticing that the location of the zero is about at $g_{m2}/g_{m3}$ times of the value $g_{m1}/C_{o1}$, we can adjust the location of the zero by changing the value of $g_{m2}$, $g_{m3}$, and the unity gain-bandwidth of the first stage. The second and feedforward stages can be designed such that the negative phase shift due to $\omega_{p2}$ is compensated by the positive phase shift of the LHP zero. When the frequency of $\omega_{p2}$ exactly coincides with that of the LHP zero, the amplifier phase margin is 90º and the unity-gain frequency is given by (3).

$$\omega_{UGBW} = A_{i2} \left( \frac{g_{m1}}{C_{o1}} \right).$$  

(3)

The effective increase in unity gain-bandwidth (UGBW) as compared to the previous reported compensation schemes is due to the fact that the dominant pole is not pushed to lower frequency, as is the case with all the pole-splitting schemes. When the LHP zero exactly cancels the non-dominant pole, a single-pole response is obtained and the phase margin is 90º. The effect of non-dominant pole of the first stage can be found by including them in calculating the transfer function given by (4). The resulting transfer function will show 3 poles and 2 LHP zeros, as shown in (5).

$$H(s) = \frac{A_{i1}}{(1+s/\omega_{p1})(1+s/\omega_{p2})}.$$  

(4)

$$H(s) = -\frac{A_{i1}A_{i2} + A_{i3}(1+s/\omega_{p1})(1+s/\omega_{p2})}{(1+s/\omega_{p1})(1+s/\omega_{p2})} \frac{(A_{i1}A_{i2} + A_{i3})(1+s/(a\omega_{p1}))}{(1+s/(b\omega_{p1}))} \frac{(1+s/(a\omega_{p1}))}{(1+s/(b\omega_{p2}))}.$$  

(5)

where $a = b = (A_{i1}A_{i2}A_{i3})/A_{i3}$.

It was observed that the number of LHP zeros created in the structure is equal to the order of the first block, but the non-dominant zero-pole doublet can usually be ignored for it lies at very high frequency. Another key constraint is that the second block should not have any non-dominant or parasitic pole before the required UGBW.

3. Effects of Pole-Zero Mismatch

One potential drawback of the proposed compensation scheme is that the increase in UGBW will not result in an equivalent decrease in settling time because of the presence of the pole-zero doublet.

Pole-zero doublet causes minor change in frequency response but may degrade the settling time based their spacing and the zero frequency$^{[6][8]}$. The effect of the pole-zero doublet on the settling time is given by (6).

$$V_{out}(t) = V(1-k_{1}e^{-\omega_{p1}t} + k_{2}e^{-\tau t}), \text { for } t>T_{s}$$  

where

$$k_{2} = \frac{\omega_{p2}^{2} - \omega_{p}}{\omega_{UGBW}^{2}},$$  

(7)

$$\tau = \frac{1}{\omega_{p2}}.$$  

(8)

and $T_{s}$ is the slewing period, $\omega_{p}$ and $\omega_{p2}$ are the doublet zero frequencies, $\omega_{UGBW}$ is the unity gain-bandwidth, and $V$ is the amplitude of step input. Equations (6), (7), and (8) indicate that for a given doublet spacing, the magnitude of the slow settling component is proportional to the doublet frequency while time constant of the slow settling component is inversely proportional to the frequency. Thus lower frequency doublet will give a response while higher frequency doublet will give a response which dies out faster but has larger amplitude. To obtain good settling time with the proposed compensation scheme, the pole-zero cancellation should occur at high frequency. The settling time also improves when the pole and zero are well matched.

4. Circuit Realization

To obtain the merit of larger output voltage swing, avoiding mirror poles, no even-order nonlinearities and rejecting the noise generated by the substrate, the fully differential architecture is employed. The first stage is a telescopic amplifier with high DC gain ensuring the high DC gain of the overall amplifier and relatively small unity gain-bandwidth. The basic differential amplifiers with a cascoding transistor to obtain higher DC gain are employed as second and feedforward stages which should not have any non-dominant pole before the overall unity gain-bandwidth. The schematic of the proposed op-amp is shown in Fig. 3.

Equations (9)-(15) show the DC gain of the three stages and the capacitors as well as resistances of the internal and external output nodes.

$$A_{i1} = g_{m1}(g_{m5}r_{ds5}r_{ds4})P_{g_{m6}r_{ds6}r_{ds1}}$$  

(9)
\[ A_2 = g_m (r_{ds} P_{r_{d10}} P_{r_{d11}}) \quad (10) \]
\[ A_3 = g_m (r_{ds} P_{r_{d10}} P_{r_{d11}}) \quad (11) \]
\[ r_{d1} = g_m (r_{ds} P_{r_{d10}} P_{r_{d11}}) \quad (12) \]
\[ r_{d2} = g_m (r_{ds} P_{r_{d10}} P_{r_{d11}}) \quad (13) \]
\[ C_{d3} = C_{d6} + C_{d7} + C_{g3} / 2 \quad (14) \]
\[ C_{d1} = C_{d8} + C_{d10} + C_{d11} + C_L. \quad (15) \]

Fig. 3. Proposed differential op-amp.

The non-dominant pole is located at \(1 / (r_{d2} C_{d2})\) and the location of the LHP zero is given by (2). The key point of the design strategy is to place them at the same frequency. Since the values of pole and the LHP zero depend on parasitic capacitances and the feedback factor, exact cancellation may not be possible. However, the effect of the pole-zero mismatch is small because the cancellation occurs at high frequency. In this work, the cancellation is arranged around the frequency 30 MHz. The transconductance of the second and feedforward stage is increased as much as possible to push the poles to high frequency.

Fig. 4. Continuous-time CMFB circuit for the first stage.

For all the three stages are fully differential, the common-mode feedback (CMFB) circuit is needed. The most commonly used CMFB structure are continuous-time CMFB and switch-capacitor CMFB. To speed up the CMFB circuit, the continuous-time CMFB is applied to the first stage while switch-capacitor CMFB schemes are employed for the second and the feedforward stages ensuring a larger output swing. The architectures of the employed CMFB circuits are shown in Fig. 4 and Fig. 5.

5. Simulation Results

Simulated by the 0.35 µm CMOS RF technology, the result is shown in Fig. 6. The DC gain is 118 dB, the unity gain-bandwidth is 1 GHz, and the phase margin is 61° with 4 pF load. The settling behavior of the op-amp is simulated by the test circuit in Fig. 7 which is the basic switched-capacitor circuit in pipeline ADC application, and the simulation result is shown in Fig. 8.

Fig. 6. Frequency response of the open-loop op-amp.

Fig. 7. Test circuit for the op-amp settling behavior.

Fig. 8. Pulse response of the close-loop op-amp.

Fig. 8 shows that the op-amp achieves a settling time better than 0.01% of accuracy at 5.8 ns. The whole performance of the op-amp is shown in Table 1. Comparisons with previous designs in [9] and [10] are also included.

6. Conclusions

Based on NMCF compensation scheme, a high-performance fully differential op-amp using the 0.35 µm CMOS RF technology has been designed which obtains high DC gain of 118 dB, high unity gain-bandwidth of 1 GHz, and good phase margin of 61°. The increase in UGBW as compared to other compensation schemes is due to the fact that the dominant pole is not pushed to lower frequency. A LHP zero is used to cancel the phase shift of the non-dominant pole to obtain a good phase margin. The pole-zero doublet is placed at high frequency to obtain fast setting performance. The simulation demonstrates that the settling time of the op-amp is 5.8 ns when achieving 0.01% accuracy. This verifies that the op-amp is suitable for the high-speed high-accuracy switch-capacitor circuits such as front-end S/H cell and the MDAC module for pipelined ADCs.

Table 1: Summarized performance of the op-amps

<table>
<thead>
<tr>
<th>Main characteristics</th>
<th>This work</th>
<th>Ref. [9]</th>
<th>Ref. [10]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply/V</td>
<td>3.3</td>
<td>3.3</td>
<td>1.2</td>
</tr>
<tr>
<td>DC Gain/dB</td>
<td>118</td>
<td>106</td>
<td>128.8</td>
</tr>
<tr>
<td>Unity Gain frequency/Hz</td>
<td>1G</td>
<td>402M</td>
<td>693M</td>
</tr>
<tr>
<td>Phase Margin/Degree</td>
<td>61</td>
<td>79</td>
<td>48</td>
</tr>
<tr>
<td>Output Swing/V</td>
<td>3</td>
<td>2.5</td>
<td>1.07</td>
</tr>
<tr>
<td>Power cons./mw</td>
<td>22</td>
<td>8.57</td>
<td>18</td>
</tr>
<tr>
<td>Load Cap/pF</td>
<td>4</td>
<td>4</td>
<td>3.2</td>
</tr>
<tr>
<td>Setting Accuracy</td>
<td>0.01%</td>
<td>0.05%</td>
<td>0.1%</td>
</tr>
<tr>
<td>Setting Time/ns</td>
<td>5.8</td>
<td>8.8</td>
<td>33</td>
</tr>
</tbody>
</table>

References


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