Guest Editorial

Special Section on Green Technologies: Energy-Efficient Circuits, Systems, and Devices

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Green technologies refer to environmentally sustainable approaches to our daily lifestyle, industry, computing, IT, and literally everything. As the enabling technology, the electronics, including circuits, systems, and devices, are the key areas of research interests in green technologies. To be green means lower power and higher energy efficiency in the user’s side and better management of energy sources in the provider’s side. In the recent several years, the energy-efficient devices, circuits, and systems have received considerable attention in both academia and industry. It has been a clear trend that it is and will continue to be an area of extensive research interests in the coming years.

In connection with the above view, and being invited by the Editor, Ms. Jasmine Xuan Xie, we have proposed this Special Section on Green Technologies: Energy-Efficient Circuits, Systems, and Devices. The focus is basically on the architecture, algorithm, implementation, and design methodology of energy-efficient circuits, systems, and devices. Meanwhile, we paid particular attention to the design of low-power integrated circuits, which determines primarily the performance of modern electronic systems and applications, and is considered as a fundamental problem in green technologies.

It is with pleasure that we have received a number of manuscript submissions; they were reviewed by expert researchers. The accepted papers cover a wide spread of topics in green electronics, including the generation, management, and consumption aspects of integrated circuits and systems.

The special section is opened by a review paper on energy harvesting systems for green computing, contributed by Prof. Terrence Mak with The Chinese University of Hong Kong. Energy harvesting is a promising alternative to battery-powered systems and provides an opportunity to achieve sustainable computing with ambient energy sources. While these devices encompass a number of non-classical system behaviors, e.g., nondeterministic power density, which prevents the effectively utilization of the harvested energy. The author investigated new design methods and tools that are used to enable power adaptive computing and, particularly, catering non-deterministic voltage, which can efficiently utilize ambient energy sources. Also, a co-optimization approach to maximize the computational efficiency from the harvested ambient energy is proposed. The paper provides an overview of these methods. Emerging technologies, e.g., 3D-IC, that enable new paradigm of green and high-performance computing are also discussed.

The next 2 papers deal with the system level aspects of energy efficient design. Hui Dong et al. presented a dynamic power consumption model, based on which they proposed the combining task scheduling for power adaptive dynamic reconfigurable systems. The idea is to exploit the ambient energy sources to supply the electronic load, where the system has to match between power supply and demand under various environments at real time. In this paper, the authors proposed a dynamic power consumption model using the lookup table as a basic unit, and established a system-level task scheduling model based on task types. The simulation result shows that the system can automatically adjust the power consumption in case the external energy input changes. The utilization portion of the system dynamic power improves from 80.05% to 91.75% during the first task assignment, while during the entire processing cycle, the total energy efficiency is a remarkable value of 97.67%.

Jun-Shi Wang et al. discussed the power estimation for FPGAs based on signal probability theory. The current power estimation tools provided by FPGA design tools use signal activity data created by logic simulation with test vectors to determine the toggle rate of each signals. The accuracy of estimation power highly depends on the quality of test vectors, and in particular, the pattern coverage. Employing probability distribution to describe the uncertainty of signals, this paper proposes an algorithm which is able to estimate FPGA power more effectively and accurately with signal probability distribution rather than test vectors.

The rest 4 papers discuss the energy-efficient design techniques for integrated circuits and systems, which are the main challenge to electronic designers.
The design of a diode type un-cooled infrared focal plane array readout circuit was presented by Prof. Li-Nan Li et al.. The diode infrared focal plane array uses silicon diodes as a sensitive device for infrared signal measurement. By the infrared radiation, the infrared focal plane can produce a small voltage signal. The traditional readout circuit structure cannot be applied to it. In this paper, a new readout circuit for a diode un-cooled infrared focal plane array is developed. The principle of detector array signal readout and small signal amplification is given in detail. The readout circuit can be applied to CMOS ROIC with an array as large as 320×240.

The next paper discusses a phase interpolator clock and data recovery (CDR) with low voltage current-mode logic (CML), and the charge pump and loop filter are replaced by a digital filter. Due to the nature of CML circuits, the CDR can operate in a low supply voltage. And the swing of the differential inputs and outputs is less than that of the CMOS logic. At a power supply voltage of 1.2 V, the static current consumption is about 20 mA. This structure also offers the benefit of increased system stability and faster acquisition.

We have two papers in this section that discuss the design of a SerDes transceiver for IEEE1394b standard in detail. At block level, Jin-Yue Ji et al. described the design of a 1-GHz charge pump PLL frequency synthesizer. The PLL’s loop dynamics are analyzed in depth and theoretical relationships among all loop parameters are clearly described. The parameters are derived and verified by a Verilog-A model, which ensures the accuracy and efficiency of the circuit design and simulation. A 4-stage ring oscillator is employed to generate 1-GHz oscillation frequency and is divided into low frequency clocks by a feedback divider. The architecture is a third-order, type-2 charge pump PLL. The simulated settling time is less than 4µs. The RMS value of period jitter of the PLL’s output is 2.1ps. The PLL core occupies an area of 0.12 mm², 1/4 of which is occupied by the MiM loop capacitors. The total current consumption of the chip is 16.5 mA. The chip has been fabricated in a 0.13 µm CMOS technology.

In the last paper, Long-Fei Wei et al. described the design of a complete multi-rate SerDes transceiver, where simple and effective pre-emphasis and equalizer circuits are used in the transmitter and receiver, respectively. A phase interpolator based clock and data recovery circuit with optimized linearity is also exploited. With an on-chip fully integrated phase locked loop, the transceiver works at data rates of 100 Mb/s, 400 Mb/s, and 800 Mb/s, supporting three different operating modes of S100b, S400b, and S800b for IEEE 1394b. The chip has been fabricated using a 0.13 µm CMOS technology. The die area of transceiver is 2.9×1.6 mm² including bonding pads and the total power dissipation is 284 mW with 1.2 V/3.3 V supply voltages.

As the guest editor of this special section, I would like to express my gratitude to all the authors, with papers accepted as well as rejected, for their generous contribution by submitting the manuscripts, and to the reviewers for their time, effort, and expertise that have enabled an efficient review process. In particular, I would like to thank Xuan for her countless effort and enormous help throughout the process.

Finally, I wish everybody a merry Christmas and happy new year of 2013.

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Qiang Li received the B.Eng. in electrical engineering from the Huazhong University of Science and Technology (HUST), Wuhan, China and the Ph.D. degree in electrical and electronic engineering from the Nanyang Technological University (NTU), Singapore. He has been working on analog/RF and mixed-signal circuits in both academia and industry, holding positions of RTP trainee, senior/research engineer, project leader, and technical consultant during 2001–2009 in Singapore. In 2009, he returned to China as a professor at UESTC, Chengdu, where he has brought up the analog group. His research interests include ultra-low voltage and micro power analog/RF & mixed-signal circuits, data converters, and digital-intensive analog design techniques.

Dr. Li was the author of 30+ scientific publications, 2 international patents and the book Analysis and Design of CMOS Ultra-Wideband Impulse Radio Transceiver (VDP/LAP Lambert Academic Publishing, June 2010). He serves as a member of Editorial Board for the International Journal of RF and Microwave Computer-Aided Engineering (SCI-indexed) and reviewer for a number of scientific publications and funding agencies. He was the recipient of the New Century Excellent Talents Program Award from the Ministry of Education of China, and Teaching Excellence Award for Young Faculty Members from UESTC.