Abstract—Energy harvesting technologies provide a promising alternative to battery-powered systems and create an opportunity to achieve sustainable computing for the exploitation of ambient energy sources. However, energy harvesting devices and power generators encompass a number of non-classical system behaviors or characteristics, such as delivering nondeterministic power density, and these would create hindrance for effectively utilizing the harvested energy. Previously, we have investigated new design methods and tools that are used to enable power adaptive computing and, particularly, catering non-deterministic voltage, which can efficiently utilize ambient energy sources. Also, we developed a co-optimization approach to maximize the computational efficiency from the harvested ambient energy. This paper will provide a review of these methods. Emerging technologies, such as 3D-IC, which would also enable new paradigm of green and high-performance computing, will be also discussed.

Index Terms—Energy harvesting, green computing, three-dimensional-integrated circuit (3D-IC) design.

1. Introduction

Recent advancements in microelectromechanical (MEMS) technology present and apply novel design and manufacturing processes that enable the integration of self-powered devices, whose energy is harvested from the environment, in micro-packages and integrated circuits. Much study has been carried out to improve the energy harvesting efficiency\(^{[1]}\)\(^{[4]}\). Such energy harvesting systems provide a promising alternative to battery-powered systems and create opportunities for architecture and design innovation for the exploitation of an ambient energy source.

Previous work on energy harvester systems focuses on individual components design. Many research groups have designed and prototyped at subsystem-level with unique interfaces and specific communication channels. Although the self-powered system can be produced by plugging together individual components, the overall system sustainability, in terms of energy utilization and computational efficiency, is relatively low. Sustainability is crucial, especially, at the era of continuing progress and massive integration in silicon technologies. Applications, such as health monitoring systems, distributed sensors, portable communication, and entertainment systems, demand high reliability and sustainability from power dissipation. Sustainable computing with good power efficiency must be addressed from various abstraction layers that include system design, processor architecture, power adaptors, and energy harvesting power sources.

Traditional battery-powered systems work under limited energy supply. For applications requiring long working duration, much effort has been devoted to energy efficient or low-power system design. With advances in energy harvesting technologies, it is possible to implement a self-powered system that harvests ambient energy from the environment. Particularly, harvesters provide a spectrum of power delivery that subjects to various environmental conditions and systematic volumes, including solar, electromagnetic, mechanical piezoelectric vibration, and so on. This enables a new opportunity to electronic architecture design and methodology innovation for the exploitation of ambient energy source. This paper reviews two design methods to handle variable voltage sources from energy harvesting devices and to optimize the ambient energy utilization for computing. Also, emerging technologies, such as three-dimensional-integrated circuit (3D-IC), and its implication on green computing will be discussed. The area of energy harvesting electronic is calling for new techniques and paradigm of design for utilizing ambient energy effectively.

2. Voltage Sensor for Variable Voltage

Dynamic adaptation is crucial to energy harvesting circuits because the harvester power efficiency can be maximized by varying the computational loads according to the scavenged energy at run-time. To achieve this goal, a sensor circuit is needed to measure the supplied power from the harvester in order to schedule activities in the computational circuity. A challenge is that this sensor needs also to be powered by the same harvester, where the power supply is either unreliable or unstable in terms of its...
voltage levels. Another problem is that stable and known voltage or current references, a prerequisite of most traditional voltage measurement devices, generally do not exist in such an operating environment. Previously, we propose an approach to voltage sensing, which we call energy-proportional. It is based on the use of a sampling capacitor, which converts power supply voltage to an amount of energy in the form of a charge stored on this capacitor, plus a charge-to-digital converter that provides reliable conversion of the stored energy to a binary code on the output. In this method, electric charge in the sampling capacitor is converted to the binary code in a single step. An asynchronous counter is designed to act as both an oscillator and a counter, thereby combining the two main functionalities in one circuit: converting charge to frequency and integrating frequency to codes. It is crucial that every signal transition in the asynchronous counter contributes to the formation of the output code from the sensor, and each such transition consumes a certain quantum of energy taken from the sampling capacitor. Thus, the switching activity and output of the counter virtually becomes proportional to the input energy “invested” into this computation. This constitutes what we call energy-proportional computing.

Fig. 1 shows a general architecture of the proposed voltage sensor circuit in a system depending on harvested energy. A sensing round starts with the charging of the sampling capacitor (\(C_{\text{sample}}\)) from the \(V_{dd}\) being sensed. The result amount of charge on this capacitor is uniformly related to the \(V_{dd}\). This capacitor’s voltage will be used as input to the asynchronous counter circuit. The capacitor is then discharged for some time by using the energy in its charge to perform some quantifiable work. The amount of work completed reflects the sampled charge (and the \(V_{dd}\) value at the time of sampling). In this design an asynchronous counter counts the pulses generated by itself to record its amount of work. The sampling circuit in Fig. 1 works in two states. In the first or charging state \(S_1\) is on and \(S_2\) is off. \(C_{\text{sample}}\) is charged to \(V_{dd} - V_{s1}\), where \(V_{s1}\) is the voltage drop across \(S_1\). This state should be long enough to fully charge the sampling capacitor \(t_{\text{charging}}\). In the second or conversion state \(t_{\text{conversion}}\) \(S_1\) is off and \(S_2\) is on. In this state \(V_{\text{in}}\) which is \(V_{dd} - V_{s1} - V_{s2}\), where \(V_{s2}\) is the voltage drop across \(S_2\), is applied to the load counter. In this design \(S_2\) is used to bypass the sampling circuit at the end of the conversion time. At this time, the counter stops counting and latches the output. Not shown in the figure, the end of conversion should also discharge \(C_{\text{sample}}\) readying it for the next sensing round.

Fig. 2 depicts the value of the output count for three different sampling capacitor values with three different output time choices \((T=t_{\text{charging}}+t_{\text{conversion}})\) over a range of voltages \((V_{dd}\in[0, 1V])\). This figure shows two slightly different slopes on each individual curve. The reason is that dramatic decrease in on to off currents \((I_{\text{on}}/I_{\text{off}})\) in subthreshold region changes the delay property of circuit.

The design of a voltage sensor for energy harvesting circuits based on a charge-to-digital converter is presented. Simple design of the proposed voltage sensor frees it up from the requirement for a stable reference voltage or current. This makes it suitable for the voltage variable environment. This voltage sensor consists of a
capacitor-based sampling circuit and an asynchronous toggle counter circuit. The binary counter works using the charge stored in the sampling capacitor which is directly related to the power from energy harvester. This counter does not require a separate clock, as it relies on the asynchronous hand-shaking protocol under the principle of semi-modular circuits\cite{6}. The handshake encodes request and acknowledgement signals for communication between modules. When the power supply varies, the signal transmission can be adjusted automatically. The key feature of this method is that the sensor is entirely powered by the energy of the charge obtained from the voltage that it measures and the speed at which it works reflects this voltage. This makes the design work towards the energy-proportional principle.

3. Power Adaptive Systems

The design criteria for systems using energy harvesting sources are fundamentally different from those using a battery. The battery-based system benefits from a relatively predictable metric of energy residual, suffices to characterize the energy availability, and is seemingly an unbounded power supply. For an energy harvesting system, rather than a limited energy supply, it has a limit on the power that the energy can be used, and the power supply from energy harvesters varies with time. Although power regulators aim to stabilise and deliver a constant power supply, there is an upper bound for the transient power delivered to the computational electronics.

In contrast to low-power circuit design principles, it is desirable that the computational load in an energy harvesting system consumes energy at an appropriate rate that is compatible with the harvester, in which the computational performance is maximized while the power consumption of the computational load is not greater than the power supplied from the harvester. Therefore, an intelligent control of the computational load that adapts the computation performance to the transient power constraints from the energy harvester is required.

We developed a two-stage design optimization approach to achieve optimized utilization of harvested energy. Specifically, at design-time, given the characteristics of the solar energy harvester, an SPMD (single process, multiple data) structure of the computational load is determined for an application, maximizing the computation speed on a target hardware platform. The parallel computation structure contains multiple homogeneous processing units (PUs), each with an enable control signal. When the system energy is sufficient, all PUs are enabled and the computation system runs at the highest speed; otherwise some of the PUs are disabled correspondingly. This can be realized using clock gating\cite{9} technique and can adjust the system power consumption.

At run-time, a convex optimization model is presented to intelligently determine which PUs are enabled at the same time (clock gating schemes), subject to the existing state of energy harvester. The convex model is customized for each specific application, resulting in fast and globally optimal solutions.

Fig. 3 shows a typical energy harvesting system. In this design, we focus on designing the adaptive computing system and developing a run-time power management method. Here, the energy source is solar energy. Apparently, the function of the energy harvester is to transfer ambient power (light) to the electrical power to supply the whole system. The power varies in a time scale of minutes. Batteries and ultra-large capacitors are two options for the energy storage. In this work, we assume that the energy storage only provides adequate energy to maintain the estimator and control system, when the harvested power is less than the least working power requirement of the computing system.

The estimation method uses the length of experiments days, sampled time, and change rate of weather and weight factor. Here we use the technique\cite{9} based on the history average data and previous data values to estimate current output. It is sensitive to the sampling frequency. Here we sampled every 5 minutes in the day\cite{8}. The power adaptive computing system is shown in Fig. 4.

The computing system executes in the SPMD structure. All PUs have the same functionality, work on different data sets, and have enable control signals (Ena in Fig. 4). The structure of each processing unit, the number of processing units, and associated local memory size are customized for a specific application. The local controller communicates with the system controller in Fig. 4, enables/disables PUs independently, and manages data transfers between global memories (Global Mem in Fig. 4) and local memories.
(Mem in Fig. 4). The dynamic power consumption of this computing system linearly varies with the number of working PUs, under the same system voltage supply and clock frequency. Therefore, clock-gating some of the PUs allows the system to adapt itself to the supplied power and thus to be used in an energy harvesting system.

The system works as follows. The sensed data are first stored in the global memories. The system controller sends messages to the energy estimator and run-time optimizer to bring them into work. The estimator estimates the supply power, and the optimizer determines a proper clock gating scheme based on the estimation. Then the system controller sends control signals to the local controller of the computation system, including a starting operation signal, input data parameters (such as image size), and clock gating signals (Ena in Fig. 4). The local controller then triggers data transfers and computation. When the computational system completes its job, the local controller sends a finish signal back to the system controller and the latter handles results. After that, the system controller starts the power estimation and run-time optimization again. The whole process is repeated. It is assumed that the power stable time interval is greater than the time required by the computation system for processing one data set. In the context of this paper, solar energy is sampled every 5 minutes, while the interval is greater than the time required by the computation system linearly varies with the number of working PUs, under the same system voltage supply and clock frequency. Therefore, clock-gating some of the PUs allows the system to adapt itself to the supplied power and thus to be used in an energy harvesting system.

Fig. 5. Power variation: (a) power variation of MAT (MAT refers to the matrix multiplication design) and (b) power variation of k-means clustering.

4. Emerging 3D-IC for Green Chips and Computing

Three-dimensional (3D) integration provides a new dimension to exploit novel geometric integration of silicon dies[10]. A variety of vertical cross-die interconnection techniques are developed. For example, the through-silicon via (TSV)[11] of 3D-IC connecting multiple die/wafer layers in a single chip provides opportunities to increase the integration capacity and also reduces the global interconnects length. Also, 3D chip is capable of integrating different technological scales and/or different technological compartments such as CMOS (complementary metal-oxide-semiconductor transistor) logics, memory, analogue sensors, and even MEMS systems by implementing them over multiple die layers.

Particularly, overall performance of multi-core systems can be significantly enhanced in a 3D architecture over conventional 2D implementations. For example, our cycle accurate simulation results demonstrate the performance improvements of 3D networks-on-chip (NoC) in term of the throughput and network saturation point when compared to the 2D-NoC. Fig. 6 (b) shows the performance gain of the 3D NoCs over 2D NoCs. The improvement increases rapidly when the number of tiles increases. The account for throughput and the saturation packet injection rate improvements is due to the smaller hops count in 3D NoCs when compared to 2D NoC[12]. Thus using 3D-NoCs, substantial performance improvements can be achieved over conventional 2D implementations.

Although NoCs demonstrates a noticeable performance improvement in 3D networks, system complexity also grows significantly with the tightly coupled vertical interconnects. Significant design efforts and considerations for run-time management include thermal effects, routing dynamics, power dissipation, and hot-spot management become necessary. We have developed an on-chip distributed dynamic-programming (DP) network[13][14] for a range of applications including optimal paths planning[15], dynamic routing[14], and deadlock detection[16].

The DP-network can readily be extended to the third dimension. It will continue to tightly couple with NoC infrastructure in each layer and with the vertical connection to connect the multiple layers. This configuration can provide short interconnections between the DP-unit and the network tile and among the neighbor DP-units. Our study in [17] demonstrated the area and power overhead of each DP-unit to implement the deadlock detection is less than 0.7% and 0.12% respectively to the router area.
5. Future Work

Energy harvesting technology enables a new research motivation for novel electronic architectures and design methodologies. Future work includes investigating the efficiency of the energy estimator, studying the detailed methodologies. Future work includes investigating the motivation for novel electronic architectures and design level.

Fig. 6. 3D architecture of a many-core system and its performance analysis: (a) a DP-network coupled to a 3D mesh NoC and (b) throughput of 3D-NoCs over 2D-NoCs for 128 nodes interconnected as a mesh 2D-NoC (16×8) and mesh 3D-NoC (8×4×4) for different network grid size\[17\].

References


