Abstract—The diode infrared focal plane array uses the silicon diodes as a sensitive device for infrared signal measurement. By the infrared radiation, the infrared focal plane can produces small voltage signals. For the traditional readout circuit structures are designed to process current signals, they cannot be applied to it. In this paper, a new readout circuit for the diode un-cooled infrared focal plane array is developed. The principle of detector array signal readout and small signal amplification is given in detail. The readout circuit is designed and simulated by using the Central Semiconductor Manufacturing Corporation (CSMC) 0.5 μm complementary metal-oxide-semiconductor transistor (CMOS) technology library. Cadence Spectre simulation results show that the scheme can be applied to the CMOS readout integrated circuit (ROIC) with a larger array, such as 320×240 size array.

Index Terms—Capacitor trans-impedance amplifier, detector array signal, diode un-cooled infrared focal plane arrays, readout circuit, small signal amplification.

1. Introduction

In the period of the late 1970s to early 1980s, the third generation un-cooled infrared focal plane array (UIRFPA) detector technology had been developed. Relative to the cooled infrared focal plane array, due to its light weight, small volume, long life, low cost, low power consumption, quick start, and good stability, UIRFPA has tremendous growth in civilian and military field.

According to the detector array produced materials, the un-cooled infrared detector array can be divided into the thermistor type, heat-capacitance type, diode type, etc.[1].

The diode detector array uses the temperature characteristics of the PN junction (diode) voltage to detect the infrared radiation intensity. This structure is compatible with modern complementary metal-oxide-semiconductor transistor (CMOS) processes[2] and very suitable for large-scale bulk manufacturing. It is a very promising infrared detector array type.

Generally, the bias and readout strategy of the readout circuit for the diode type UIRFPA may be divided into two types, namely, constant bias current–voltage readout and constant bias voltage–current readout. The scheme of constant bias voltage is the most used, which allows the current difference to integrate with an amplifier configured as a capacitive trans-impedance amplifier. A lot of readout circuit structures have been developed for this scheme[3]. For the constant bias current scheme, though it is not easy to design a stable constant current source, it has the maximum sensitivity. But the corresponding readout circuit structure has not been further researched, so it has positive significance to design the related readout circuit.

In this paper, a readout circuit structure is developed for the diode-type UIRFPA of constant bias current scheme. In the next section, the detector array signal readout principle is introduced. In section 3 the designed readout architecture is described. Section 4 provides experimental results and conclusions are drawn in Section 5.

2. Principle of Detector Array Signal Readout

Before discussing the diode-type UIRFPA detector readout circuit structure, it is necessary to discuss the principle of detector array signal readout. How to read the weak signal effectively and accurately is one of the keys in the circuit design and determining the readout circuit structure.

In conditions of constant current density, the forward voltage drop of the PN junction is a negative temperature characteristic[4], the PN junction voltage drop decreases with the temperature increasing as shown in Fig. 1.

Diode-type UIRFPA detectors use the temperature characteristic of semiconductor PN junction. In constant forward current conditions, if the ambient temperature changes, the forward voltage drop will accordingly change. By detecting and processing the detector array for each pixel change in voltage, the imaging of infrared radiation source can be obtained[5][6].
Fig. 1. Diode voltage temperature characteristic curve.

Fig. 2. Schematic of detector array signal readout.

However, the sensitivity of single PN junction temperature is limited, which is only about −1.3 mV/K to −2 mV/K\(^7\)\(^8\). In order to increase the signal to noise ratio of the infrared detector output signal, six PN junction diodes are in series as a detector pixel. By inrushing constant current, under different infrared radiation, it can produce approximately a 0.5 mV to 5 mV voltage change.

Let some pixels in the detector array be covered so that they can not accept the irradiation from the infrared radiation source, but the other pixels be normally irradiated by the infrared radiation source. With inrush constant current, the forward bias voltage generated by the covered pixel does not change with the change of the infrared radiation source, but that of the uncovered pixel produces different positive bias with the different intensity of the infrared radiation. We let the forward bias voltage \(V_{ref}\) generated by the covered pixel be the reference, and those of other un-covered pixels, such as \(V_1, V_2, \ldots, V_n\), subtract the reference \(V_{ref}, V_1-V_{ref}, V_2-V_{ref}, \ldots, V_n-V_{ref}\) are the effective signal generated by the detector array (shown in Fig. 2).

It can be seen from the above analysis that the detector signal readout needs a specific readout circuit structure. The main purpose of this paper is to discuss a new readout circuit structure for reading out the corresponding voltage value generated by the infrared radiation, which indirectly reflects the size of the temperature of the detector components and infrared radiation.

3. Readout Circuit Architecture

For the infrared focal plane CMOS readout circuit, the readout circuit is mainly composed of the small signal amplification, timing control section, analog to digital converter part, rear uniformity correction, and display circuit part.

This paper mainly discusses the small signal amplification part.

The main readout techniques contain direct injection (DI), current mirror integration (CMI), capacitor trans-impedance amplifier (CTIA), and so on\(^3\). By the basic circuit forms, some new readout circuit structure can also be derived through certain combination of changes. However, the integration linearity of DI circuit will incline significantly when the input signal range is wide. In CMI, the CMOS transistors work at sub threshold area if the input signal is too small, which causes the structure instability and inaccuracy. On the contrary, CTIA can achieve wide detecting range and good integration linearity. These properties make the capacitive feedback trans-impedance amplifier structure applicable to the array detector with an increasing scale.

Thus, this paper presents a small signal amplification structure based on the traditional CTIA for a 320×240 size array.

The schematic of CTIA is shown in Fig. 3, where the integration capacitor (\(C_{int}\)) is placed on the feedback loop of the amplifier with a reset device \(S_{res}\) to discharge the integration capacitor and reset the amplifier output to the reference voltage. The detector bias is also controlled through the virtual-short feature of the amplifier. Thus, good detector-bias control can be obtained in the CTIA. Due to the Miller effect on the integration capacitor, its capacitance can be made extremely small to obtain low noise and high-sensitivity performance.

Because the infrared detector array outputs in voltage signals, it cannot directly apply to CTIA, so a trans-conductance amplifier (GM AMP) is required to convert the voltage signal into current signal. The schematic of small signal amplification is shown in Fig. 4.
As shown in Fig. 4, injecting the 20 μA benchmark current into the detector array, then the small voltage signal generated by uncovered and covered pixels are $v_{signal}$ and $v_{signal_ref}$, respectively. As the input signal of the small signal amplification, these two signals are connected to the two inputs of the trans-conductance amplifier, respectively. The GM AMP will convert the difference of two input signals to a current signal, and integrate on the integration capacitor $C$. Integration capacitor $C$ is in parallel with a switch, which is used to reset of the integrating amplifier, so that the integrating amplifier can be continuously integrated for each pixel signal. As an external reference voltage, $V_{ref}$ is used to determine the potential when integrating amplifier is cleared (when the integral clear switch $S$ is closed).

The equivalent input signal of the integrating amplifier is $v_{in} = v_{signal} - v_{signal_ref}$. The current signal that is converted by GM AMP is $i = g_m v_{in} = g_m (v_{signal} - v_{signal_ref})$, where $g_m$ is the trans-conductance value of GM AMP. When the integrating amplifier is reset, the output voltage $V_{out} = V_{ref}$, when the integrating amplifier is in the amplification status (integral clear switch $S$ is disconnected), the relationship between the output voltage and the voltage of the integration capacitor $v_c$ is $V_{out} = V_{ref} - v_c$, that is:

$$V_{out} = V_{ref} - \frac{1}{C} \int_{t_1}^{t_2} g_m v_{in} \, dt.$$  \hspace{1cm} (1)

If the integration time in each cycle is $T$, at the end of each integral cycle, the output voltage signal is

$$V_{out} = V_{ref} - \frac{1}{C} \int_{t_1}^{t_2} g_m v_{in} \, dt.$$  \hspace{1cm} (2)

where $\bar{V}_{in}$ is the average of the input signal in integration time $T$. And then the magnification of the integrating amplifier is

$$A = \frac{V_{out} - V_{ref}}{\bar{V}_{in}} = -\frac{g_m T}{C}.$$  \hspace{1cm} (3)

The following is the analysis of the circuit situation considering the array detector input noise.

The equivalent input signal is $v'_{in} = v_{in} + v_{noise}$, where $v_{noise}$ represents high frequency random noise in the input signal, and $\bar{V}_{noise}$ is the average of high frequency random noise in the input signal during integration time $T$. So, in the integration time $T$, the output voltage is

$$V'_{out} = V_{ref} - \frac{1}{C} \int_{t_1}^{t_2} g_m v'_{in} \, dt = V_{ref} - \frac{1}{C} \int_{t_1}^{t_2} g_m (v_{in} + v_{noise}) \, dt.$$  \hspace{1cm} (4)

At the end of each integral cycle, the output voltage signal is

$$V'_{out} = V_{ref} - \frac{G_m \bar{V}_{noise} T}{C} - \frac{G_m \bar{V}_{in} T}{C}.$$  \hspace{1cm} (5)

It can be known that for a long period of integration time, the average of the high-frequency random noise is approximately equal to zero, that is $\bar{V}_{noise} = 0$ and then the magnification of the integrating amplifier is

$$A = \frac{V'_{out} - V_{ref}}{\bar{V}_{in}} = -\frac{G_m T}{C}.$$  \hspace{1cm} (6)

It can be seen that considering the input noise of the detector array, not only the input signal can be amplified, but also the high frequency random noise can be filtered out by small signal amplification.

A simple differential-input-to-single-output amplifier is used as the GM AMP as shown in Fig. 5. The difference voltage between $v_{signal}$ and $v_{signal_ref}$ is amplified and converted into current at the node $I_{out}$ by the GM AMP. In this circuit, two currents are generated by the basic differential pair, the difference of this two current is obtained by using the three current mirrors, and finally get the needed current. The detector voltage signal is very small, so by using the simple differential pair, a current with good linearity can be obtained. The output current is

$$I_{out} = G_m v_{in} = G_m (v_{signal} - v_{signal_ref}).$$  \hspace{1cm} (7)

The amplifier is the core unit module in the amplifier circuit, whose performance directly determines the amplifier circuit’s performance, so the design of core amplifier and reasonable adjustment of the amplifier parameters are the keys in the readout circuit design. For the operational amplifier (OTA), we use the folded-cascode operational amplifier (OP AMP) structure, as shown in Fig. 6, which generally does not require frequency compensation and can provide a large gain and wide bandwidth, as well as a good supply voltage rejection ratio and large output swing.
Fig. 5. Circuit of a simple differential-input-to-single-output amplifier using as GM AMP.

Fig. 6. Schematic of fold-cascode OP AMP.

4. Simulation Results

The simulation of proposed circuit is based on CSMC (Central Semiconductor Manufacturing Corporation) 0.5 μm standard process technology. For a 320×240 detector array, the entire readout circuit is working in the way that every time one pixel signal is processed. For timing selection circuit is simple, it is not described in detail here.

The simulation results of GM AMP are illustrated in Fig. 7 with variable input voltage. The differential voltage pair is connected to the input of the trans-conductance amplifier and the input signal cycle is 200 ns. It can be seen from the simulation results that the output current and input voltage are in a linear relationship, which provides a good foundation for the further processing of the signal.

The simulation result of the small signal amplification circuit is given in Fig. 8. The architecture of amplification is illustrated in Fig. 4, and the parameters of the small signal amplification circuit are listed in Table 1.

It can be seen from Fig. 8 that the linear small signal is input, the amplifier can well integrate and enlarge the small signal, and a good linear relationship between output and input signals is presented in the graph. The magnification is about 200. This result can meet the actual demand.

5. Conclusions

A readout circuit for an UIRFPA has been designed.
based on the traditional structure of CTIA. The circuit is composed of a GM AMP and CTIA. The GM AMP uses the basic differential pair to convert the voltage signal into the current signal with a simple structure and good performance. OTA is fold-cascode, which is a compromise on the power and performance. The function of the circuit is simulated by the CSMC 0.5 μm CMOS technology library and the simulation results of experiment meet the functional requirements. This circuit can also apply to the use of a larger array structure by adjusting the integration time and the integration capacitor appropriately.

References


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