Discrete-Time Chaotic Circuits for Implementation of Tent Map and Bernoulli Map*

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Abstract Discrete-time chaotic circuit implementations of a tent map and a Bernoulli map using switched-current (SI) techniques are presented. The two circuits can be constructed with 16 MOSFET's and 2 capacitors. The simulations and experiments built with commercially available IC's for the circuits have demonstrated the validity of the circuit designs. The experiment results also indicate that the proposed circuits are integrable by a standard CMOS technology. The implementations are useful for studies and applications of chaos.

Key words chaotic circuit; switched-current; tent map; Bernoulli map

In recent years, chaotic signals with the characteristics of broadband, unpredictability and inherent randomness open up new promising vistas in the field of communication systems, signal processing systems and improving system EMC, etc.[1,2]. Thus, much interest has been attracted to the study of the chaotic systems. In the field of engineering, many types of the chaotic circuits have already been reported[3~10], such as monolithic Chua's circuit[5], discrete-time chaotic circuits[6~9].

For a practical chaotic circuit, it should have a simple structure and can be integrable with a standard IC technology. In this paper, we proposed two types of the discrete-time chaotic circuits for implementation of tent map and Bernoulli map. Both the chaotic circuits are based on switched-current (SI) techniques. The number of MOSFET'S used in the proposed circuits are less than that used in Ref.[6]. The simulation and experiment results have confirmed the validity of the circuit designs.

1 Circuit Structures

Fig.1 shows the generation of the discrete-time chaotic signal using piecewise linear map. During one clock phase, the output of the sample and hold stage (S&H), , is connected to the input of the nonlinear map g. The corresponding output signal is

\[ X_n = g(X_{n-1}) \]  

Simultaneously, the output signal \( X_n \) is sampled. In the next clock phase, the sampled \( X_n \) is connected to the input of the map g, as next \( X_{n+1} \). The chaotic signal sequence \( X_s \) after dealing is applied to the systems to be considered. The piecewise linear map \( g \) can be a tent map or a Bernoulli map, etc. The following will describe how to use the two nonlinear maps for the design of the discrete-time chaotic circuits separately.

1.1 Tent Map

Fig.2(a) shows the proposed tent-map chaotic circuit. The synthesis of this chaotic circuit using SI technique is based on the equation of the tent map

\[ X_{n+1} = 2 \left[ X_n - (2X_n \Theta 1) \right] \]

\[ \begin{cases} 2X_n & 0 \leq X_n < \frac{1}{2} \\ 2 - 2X_n & \frac{1}{2} \leq X_n \leq 1 \end{cases} \]  

(2)

where \( \Theta \) is the bounded-difference operator defined as

\[ x \Theta y = \begin{cases} x - y & x > y \\ 0 & x \leq y \end{cases} \]

For Eq.2, the reference current source \( I_1 \) in Fig.2(a) is normalized as 1 and the scope of the chaotic current signal is normalized within \( X_s \in [0,1] \), so the value of
the current $I_1$ determines the scope of the chaotic current signal. From Fig.2(a), we can find that the discrete-time chaotic circuit is composed of the tent map circuit and the S&H circuit. To realize this circuit, the key technique is current mirror. The numbers at the MOSFET's shown in Fig.2(a) are the current-copying ratios of the current mirrors, namely, the normalized $W/L$ ratios of the MOSFET's. In this circuit, the operation $2X_n \Theta 1$ is realized by the bounded-difference circuits composed of the NMOS current mirrors. The output of the tent map circuit is delayed one clock and is fed back to the input.

$$\begin{align*}
2X_n & \quad 0 \leq X_n < \frac{1}{2} \\
2X_n - 1 & \quad \frac{1}{2} \leq X_n \leq 1
\end{align*}$$

(3)

where $u(\cdot)$ is the unit step function.

For Eq.(3), the reference current source $I_2$ in Fig.2(b) is normalized as 1/2 and the scope of the chaotic current signal is normalized within $X_n \in [0,1]$, therefore the value of the current $I_2$ determines the scope of the chaotic current signal. From Fig.2(b), we can see that the discrete-time chaotic circuit is composed of the Bernoulli map circuit and the S&H circuit. The numbers at the MOSFET's shown in Fig.2(b) are the current-copying ratios of the current mirrors. In this circuit, the operation $u(X_n - 0.5)$ is realized with the current comparator composed of the switch $S$ and the NMOS and PMOS current mirrors. The other circuits are the same as those in the tent map chaotic circuit.

1.2 Bernoulli Map

Fig.2(b) shows the proposed Bernoulli map chaotic circuit. The synthesis of this chaotic circuit using SI technique is based on the equation of the Bernoulli map

$$X_{n+1} = 2X_n - u(X_n - 0.5) =$$

![Fig.2 Discrete-time chaotic circuits](image)

![Fig.3 Simulation results](image)

2 Simulation Verification

To confirm the validity of the circuit designs, the simulations for the circuits are performed according to the proposed circuits shown in Fig.2. The simulation conditions are as follows

Reference Current Source $I_1$: 50 $\mu$A
Reference Current Source $I_1$: 25 μA
Switching frequency of $\phi$ and $\bar{\phi}$: 10 kHz
Capacitance of $C_1$ and $C_2$: 500 pF

Fig. 3 and Fig. 4 show the results obtained by our simulations. Fig. 3(a) is the simulated tent map function, and Fig. 3(b) is the simulated chaotic signal waveform of the tent map. In the same way, Fig. 4(a) and (b) are the simulated Bernoulli map function and the simulated chaotic signal waveform of the Bernoulli map, respectively. Note that during simulating an impulsion must be fed to the chaotic circuit to make it operate normally for the ideal characteristic of the software simulation environment.

3 Experimental Verification

Experimental verifications have been performed. The experimental circuits are built with commercially available IC, CD4007UB, and discrete bipolar transistor, S8550. The bipolar transistor is used to realize the reference current source $I_1$ and $I_2$. The experimental conditions are as follows:
Reference Current Source $I_1$: 50 μA
Reference Current Source $I_2$: 25 μA
Switching frequency of $\phi$ and $\bar{\phi}$: 1.5 kHz
Capacitance of $C_1$ and $C_2$: 2.2 nF

Fig. 5(a) shows the tent map function, and Fig. 5(b) shows the chaotic signal waveform of the tent map obtained in the experiments. Fig. 6(a) and (b) show the
Bernoulli map function and the chaotic signal waveform of the Bernoulli map obtained in the experiments, respectively. In these experiments, all the chaotic current signals are detected by 20kΩ resistance and measured by TDS3012 oscilloscope. Because noise exists in these experiments, an initial impulse signal does not need to feed to the chaotic circuit.

4 Conclusions

Two types of the discrete-time chaotic circuits for implementation of a tent map and a Bernoulli map are presented in this paper. The syntheses of these chaotic circuits are based on SI techniques. The proposed circuits can be constructed with 16 MOSFET's and 2 capacitors. The simulation and experiment results demonstrated the validity of the circuit design. The experiment results also indicated that the proposed circuit is integrable by a standard CMOS technology. Further study will focus on improving EMC problems of the switching converters that use these chaotic signals.

References


Brief Introduction to Author(s)

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