A Fast $\pi/4$-DQPSK Demodulation Arithmetic and Realization

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Abstract  The modulated signals of $\pi/4$-DQPSK can be demodulated with the differenced method, and the technology has been used in the communication. The traditional demodulated method needs a lot of calculation. In this paper, a new method based on fast arithmetic digital demodulation of DQPSK is presented. The new method only uses the sign of the modulated signal instead of digital signal through the A/D in the traditional method. With the new method, the system has higher speed, and can save some hardware in the FPGA. An experiment of the new method with the DQPSK is given in this paper.

Key words  $\pi/4$-DQPSK;  difference demodulation;  FPGA;  MATLAB;  BER

The modulation of $\pi/4$-DQPSK ($\pi/4$ shift differentially encoded quadrature phase shift keying) is more efficient in frequency, simpler in demodulation, and more useful in communication of moving system. At present, its realization, specially, its digital circuit realization has become a hot point to be researched. Some papers have introduced the method and circuit of QPSK in digital way, for example, the QPSK are made with DSP and FPGA $[1$-$6]$. A DQPSK modulation and demodulation based on FPGA are introduced, and a new method is presented in this paper. The new method is easy to realize on FPGA and get higher speed and the same capability in anti-interference as others. With the new demodulation method, the mode of parallel operation can be applied on FPGA, so it can work faster but needs less space on FPGA. Additionally, in real circuit, the A/D converter of 1 bit can be instead of the comparer, and the hardware circuit is simpler.

1  The Demodulation of DQPSK

The modulated signal of $\pi/4$-DQPSK has only 4 different phases, $\pm \pi/4$ and $\pm 3\pi/4$, and the relation between the inputs signal and the phases is shown in Tab.1. The $\Delta\Phi$, phase jump of the carrier frequency, has included all information, and it can be demodulated by the differencing the phase.

Tab.1  The digital signals and modulating phases

<table>
<thead>
<tr>
<th>I</th>
<th>Q</th>
<th>$\Delta\Phi$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>$-3\pi/4$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>$3\pi/4$</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>$-\pi/4$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>$\pi/4$</td>
</tr>
</tbody>
</table>

Fig.1  The demodulation scheme
The scheme of the demodulation of DQPSK is shown in Fig.1. Let the mid-frequency signal be
\[ s(t) = \cos(2\pi ft + \phi) \]  
(1)
the sampling frequency of A/D is \(1/T_s\), and the output of A/D is
\[ y(nT_s) = \cos(2\pi fn + \phi_1) \]  
(2)
By normalizing
\[ y(n) = \cos(2\pi fn + \phi_1) \]  
(3)
The signal is processed through two paths, one is delayed \(T\), and the other is de-phased \(-\pi/2\), as shown in Fig.1
\[ x' = \cos(2\pi fn + \phi_1) \cos(2\pi fn + \phi_{-1}) \]  
(4)
\[ y' = \sin(2\pi fn + \phi_1) \cos(2\pi fn + \phi_{-1}) \]  
(5)
After low pass, the output is
\[ x = \cos(\phi - \phi_{-1}) = \cos \Delta \phi \]  
(6)
\[ y = \sin(\phi - \phi_{-1}) = \sin \Delta \phi \]  
(7)
where \(\Delta \phi = \phi_{-1}\), because there are only 4 phase changes, \(\pm \pi/4\) and \(\pm 3\pi/4\), in the modulated signal, there are also only 4 possibilities for output of the \(x\) and \(y\). The signal is demodulated through the judgment and parallel/serial converter. The judgment is shown in Tab.2.

<table>
<thead>
<tr>
<th>(\Delta \phi)</th>
<th>(x)</th>
<th>(y)</th>
<th>(I)</th>
<th>(Q)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(-3\pi/4)</td>
<td>-0.707</td>
<td>-0.707</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(3\pi/4)</td>
<td>-0.707</td>
<td>0.707</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>(\pi/4)</td>
<td>0.707</td>
<td>-0.707</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>(\pi/4)</td>
<td>0.707</td>
<td>0.707</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

2 The Different Demodulation of 1 bit Mid-Frequency

The different demodulation of the 1 bit mid-frequency is not the same as the old different demodulation. The modulated signal may be only sign, which can decrease the effect of varying module of the signal, and make the circuit more simply, for example, in the digital low pass filter, the multiplication may be instead of addition, so it may save space of FPGA.

For the 1 bit demodulation, the mid-frequency signal is still
\[ s(t) = \cos(2\pi ft + \phi) \]  
(8)
definite
\[ \text{sign}(x) = \begin{cases} 1 & x \geq 0 \\ -1 & x < 0 \end{cases} \]  
(9)
Let the sampling frequency of the A/D be equal to signal frequency, and the accuracy be 1 bit, as shown in Fig.1. It can be shown as a sign function, \(\text{sign}()\), in a real circuit, the output of 1 bit A/D is
\[ y(t) = \text{sign}[\cos(2\pi ft + \phi_1)] \]  
(10)
\[ x' = \text{sign}[\cos(2\pi ft + \phi_1)] \times \text{sign}[\cos(2\pi ft + \phi_{-1})] \]  
(11)
so the sin wave signal convert to the rectangle signal, and it can also be shown as
\[ x' = \sum_{n=-\infty}^{\infty} \text{Sa}(n\pi / 2) e^{j(n\pi f_0 + n\phi_1)} \sum_{n=-\infty}^{\infty} \text{Sa}(n\pi / 2) e^{j(n\pi f_0 + n\phi_{-1})} = \]  
\[ = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} \text{Sa}(mp / 2) \text{Sa}(n\pi / 2) e^{j(m\pi f_0 + n\phi_1)} e^{j(n\pi f_0 + n\phi_{-1})} \]  
(12)
After the low pass filter
\[ x = \sum_{n=-\infty}^{\infty} \text{Sa}(n\pi / 2) e^{j(n\pi f_0 - \phi_{-1})} = \]  
\[ \sum_{n=1}^{\infty} 1/(2n - 1)^2 \cos[(2n - 1)\Delta \phi] \]  
(13)
and
\[ y = \sum_{n=1}^{\infty} 1/(2n - 1)^2 \cos[(2n - 1)(\Delta \phi - \pi / 2)] \]  
(14)
The output of \(I\) and \(Q\) can be decided by the \(x\) and \(y\) as shown in Tab.3. The output is the same as shown in Tab.2. So the new method of the 1 bit demodulation is possible. It can be understood from the Fig.2. The line “--” is the traditional demodulation, and the “*” is the 1 bit demodulation. If the errors of phase is under \(\pi/4\), the sign do not change, and the output also do not mistake.
### Tab.3 The modulating phase, outputs of filters and signals

<table>
<thead>
<tr>
<th>$\Delta \Phi$</th>
<th>$x$</th>
<th>$y$</th>
<th>$I$</th>
<th>$Q$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-3\pi/4$</td>
<td>$&lt;0$</td>
<td>$&lt;0$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$3\pi/4$</td>
<td>$&lt;0$</td>
<td>$&gt;0$</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$-\pi/4$</td>
<td>$&gt;0$</td>
<td>$&lt;0$</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$\pi/4$</td>
<td>$&gt;0$</td>
<td>$&gt;0$</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

For the calculation simply, let the normalizing variance be qual to 1. The BER of the receiving signal can be calculated at different input signal energy, and the simulation on MATLAB is shown in Fig.3. ("--" is BER on theory, "*" is BER on sign, "o" is BER on 1bit).

### 4 Simulation

The anti-interference is simulated. The random of 7 bits is added in the 8 bits input modulated signal, and the noise is a half of the signal, $S/N$ is 6 db. 1 bit signal, only sign is input the demodulation. The simulation is shown in Fig.4. D_2 is 13 bits PN codes, sham random signal, to be input the circuit. MYQOUT is recovered signal and MYQCLK is recovered clock. MYI and MYQ are demodulated signal $I$ and $Q$, and the wave is shaped. When the WORKING is 1, $I$ and $Q$ are judged. If there are errors, ERROR will be 1. There are no errors after sync, and the simulation run up to 2000 bits, and the parts are shown in Fig.4.

### 5 Experiment

The signal is 8 Kb/s, and the mid-frequency is 455kHz. The xc2s100 made in XILINX Company is used. Its 60% space is used. Under the silencing, there is no error that measured condition is using 13 bits PN code. For estimating the effect, there are some differences between modulation frequency and demodulation frequency. If $|\nu|<100$ Hz, the system can work. If $|\nu|>200$ Hz, the system is wrong.

(Continued on page 86)